



CO-DESIGN & SIMULATION OF IMEC SIGEMEMS TECHNOLOGY & TSMC 0.18 CMOS USING COVENTOR MEMS+[®]/CADENCE VIRTUOSO

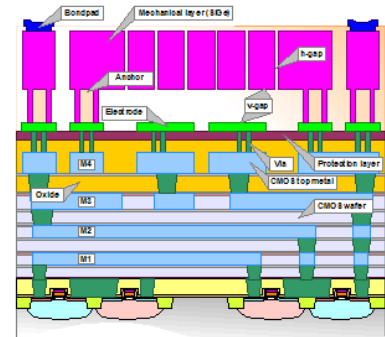
September 21-23, 2011

ABSTRACT

This three day training course aims to introduce the attendees to imec SiGeMEMS technology, the first publicly accessible technology (through [EUROPRACTICE MPW](#)s) to offer integration with CMOS circuits. The technology related component of the course therefore deals with the actual MEMS technology on one hand, but it also addresses its integration with TSMC CMOS circuits on the other hand.

A second goal of the training is to introduce participants to Coventor software tools for MEMS design. This software related component of the course focuses on Coventor MEMS+ for MEMS design. SEMulator3D for “virtual fabrication” is, however, also addressed.

The software and technology related components of the course converge on the third day, when the attendees will run a DRC and subsequently gain understanding of DRC-violations by means of virtual fabrication in SEMulator3D.



TARGET AUDIENCE

The course is aimed at postgraduate students, researchers and engineers that consider performing a MEMS-design in imec SiGeMEMS technology or by means of Coventor design software. Both experienced and inexperienced designers from both academia and industry are welcome to join. Note that some legal formalities (Design Kit License Agreement, Non-Disclosure Agreement) need to be fulfilled prior to registration.

OBJECTIVES

- ▶ Get introduced to imec SiGeMEMS technology and its integration with TSMC CMOS circuits.
- ▶ Get hands-on experience on Coventor MEMS+.
- ▶ Get to know the design-rules for SiGeMEMS technology to design with confidence.
- ▶ Get hands-on experience in “virtual fabrication” with Coventor SEMulator3D.

PROGRAM

Day 1

- ▶ Overview of SiGeMEMS technology.
- ▶ Overview of Coventor software for MEMS design.
- ▶ Presentation of the EURO PRACTICE IC-service and how to participate in an MPW-run.

Day 2

- ▶ Coventor MEMS+ hands-on session for MEMS-only design in SiGeMEMS technology.
- ▶ Coventor MEMS+ hands-on session on cosimulation of a MEMS device with CMOS in Cadence.

Day 3

- ▶ Design rules for SiGeMEMS technology.
- ▶ Hands-on design rule checking for SiGeMEMS technology.
- ▶ Hands-on “virtual fabrication” of MEMS in Coventor SEMulator3D.

LOCATION

The course is organized at imec, Leuven, Belgium. Refer to http://www2.imec.be/be_en/about-imec/offices/how-to-reach-imec-belgium.html for directions (address: imec, Kapeldreef 75, B-3001 Leuven, Belgium).

Imec performs world-leading research in nano-electronics; it also extends CMOS processes with new processing steps. Under the name CMORE, imec offers heterogeneous integration services to the industry. CMORE services range from development-on-demand, over prototyping, to low-volume production. The imec SiGeMEMS offering is part of its CMORE program.



FEES

The training is free of charge. The number of participants is, however, limited to 22. Therefore, registration is required. Do not make any travel arrangements before you get confirmation of your registration.

ACCOMMODATION

Participants need to make their own accommodation and travel arrangements. A full overview of hotels in Leuven can be found at <http://www.leuven.be/en/tourism/staying-over/hotels/>.

REGISTRATION

Because of the confidential nature of some of the training's contents, the institutes or companies of the participants are required to sign both the Design Kit License Agreement (DKLA) for imec SiGeMEMS technology (http://www.europactice-ic.com/MEMS_dkla_imec_SiGeMEMS.php) and the Non-Disclosure Agreement (NDA) for 0.18um TSMC technology (http://www.europactice-ic.com/nda_TSMC.php) in the frame of the EURO PRACTICE-IC service. Registration for this training is performed by e-mail to training@imec.be.

The number of participants is limited to 22. Do not make any travel arrangements before you get confirmation of your registration. Necessary course material will be provided.